

LOW POWER MONOLITHIC TTL ELEMENT

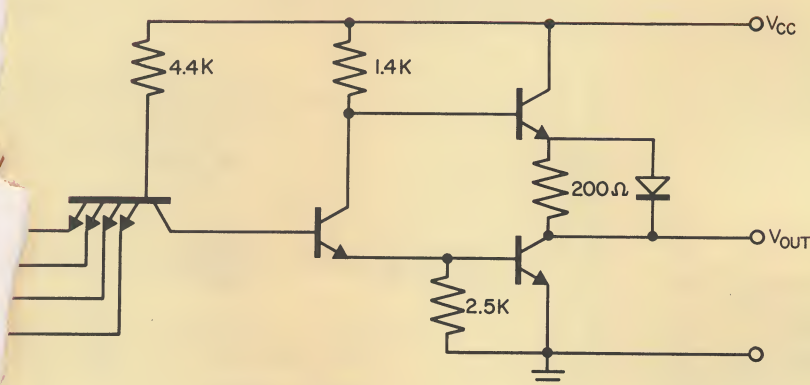
NAND/NOR GATE DRIVER

NE455J is a monolithic semiconductor integrated circuit designed for use in low power digital systems. This element is functionally identical to the SE455J. Full MIL range systems may be economically breadboarded using the NE455J element so long as the designer takes cognizance of the temperature differential. For GSE designs or other limited temperature range applications, the NE455J offers the opportunity to exploit, at very low cost, all of the major advantages of the SE455J. For additional data on the NE455J, see the SE455J data sheet.

The same planar and epitaxial techniques used in fabricating the SE400J-Series elements are employed in making the NE400J-Series. These elements are tested under Signetics established SURE Program (Systematic Uniformity and Reliability Evaluation), as described in Bulletin No. 5001. Acceptance Test Sub-Groups called out in the tabular data refer to selection and test criteria as specified in Table II of SURE Program Bulletin No. 5001. Please note, however, that the NE400J-Series is intended for operation in the 0°C to +70°C range.

CIRCUIT SCHEMATIC

NOTE: 1/2 of NE455J shown. Component values are typical.

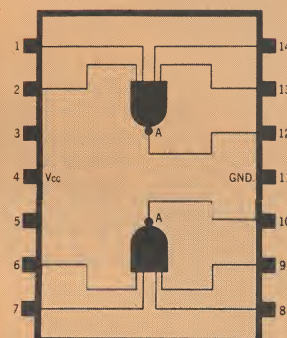


ABSOLUTE MAXIMUM RATINGS

VOLTAGE	6.0V	OPERATING TEMP.	0°C to +70°C
VOLTAGE	6.0V	STORAGE TEMP.	-65°C to +150°C
CURRENT	±10mA	θ JUNCTION TO CASE	0.2°C/mW
OUTPUT CURRENT	±100mA	JUNCTION TEMP.	150°C

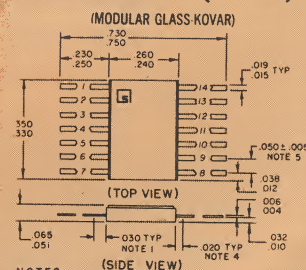
are limiting values above which serviceability may be impaired.

NE455J



NOTE:
(1) A — Active pull-up

J-PACKAGE—(TO-88)



NOTES:

- (1) Recommended minimum offset before lead bend.
- (2) All leads weldable and solderable.
- (3) All dimensions in inches.
- (4) Lead spacing dimensions apply to this area only.
- (5) Spacing tolerances non-cumulative.

ELECTRICAL CHARACTERISTICS (Notes: 1, 2, 3, 4, 5, 6)

ACCEPTANCE TEST SUB-GROUP	CHARACTERISTIC	LIMITS				TEST CONDITIONS					
		MIN.	TYP.	MAX.	UNITS	TEMP.	V _{cc}	DRIVEN INPUT	OTHER INPUTS	OUTPUTS	NOTES
A-5	"1" OUTPUT VOLTAGE	2.5			V	0°C	4.0V	0.8V		-400μA	
A-3		2.5			V	+25°C	4.0V	0.8V		-400μA	
A-4		2.5			V	+70°C	4.0V	0.8V		-400μA	
A-5	"0" OUTPUT VOLTAGE			0.32	V	0°C	4.0V	1.7V	1.7V	16mA	
A-3				0.32	V	+25°C	4.0V	1.7V	1.7V	16mA	
A-4				0.32	V	+70°C	4.0V	1.7V	1.7V	16mA	
C-1	"0" INPUT CURRENT			-1.2	mA	0°C	4.0V	0V	4.0V		
A-3				-1.2	mA	+25°C	4.0V	0V	4.0V		
C-1				-1.2	mA	+70°C	4.0V	0V	4.0V		
A-4	"1" INPUT CURRENT			20	μA	+70°C	4.0V	4.0V	0V		
A-3				10	μA	+25°C	4.0V	4.0V	0V		
	PAIR DELAY (Figure 1)		55		ns	+25°C	4.0V			DC F. O. = 20	
A-6	OUTPUT FALL TIME (Figure 2)			75	ns	+25°C	4.0V			AC F. O. = 8	10
	INPUT CAPACITANCE		3.0		pf	+25°C	4.0V	2.0V			7
	AVERAGE POWER CONSUMPTION PER GATE		9.0		mW	+25°C	4.0V				12
	"1" NOISE MARGIN DC	0.8			V	0-70°C	4.0V				11
	"0" NOISE MARGIN DC	0.48			V	0-70°C	4.0V				11
A-2	INPUT VOLTAGE RATING	6.0			V	+25°C	4.0V	50μA			9, 11
	DC FAN-OUT	20									10
	AC FAN-OUT	8									

NOTES:

- (1) All voltage and capacitance measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.
- (2) All measurements are taken with Pin 11 tied to zero volts.
- (3) Positive current flow is defined as into the terminal referenced.
- (4) Positive NAND Logic definition: "UP" Level = "1", "DOWN" Level = "0".
- (5) Precautionary measures should be taken to ensure current limiting in accordance with maximum ratings should the isolation diodes become forward biased.
- (6) Measurements apply to each gate element independently.
- (7) Capacitance as measured on Boonton Electronic Corporation Model 75A-S8 Capacitance Bridge

- (8) or equivalent, $f = 1 \text{ MHz}$, $V_{ac} = 25 \text{ mV}_{\text{rms}}$. All pins not specifically referenced are tied to ground for capacitance tests.
- (9) Output leakage current is supplied through a resistor to ground.
- (10) DC fan-out is defined in terms of a SIGNETICS Standard Unit Load, which is an NE480J gate input or an equivalent impedance.
- (11) One AC fan-out is defined as equivalent to one clock pulse input of an NE424J or a 50 pf capacitance load.
- (12) This is not a test point, but is guaranteed as a result of calculations using guaranteed test points.
- (13) Measured at 50 percent duty cycle.

FIGURE 1 — PAIR DELAY

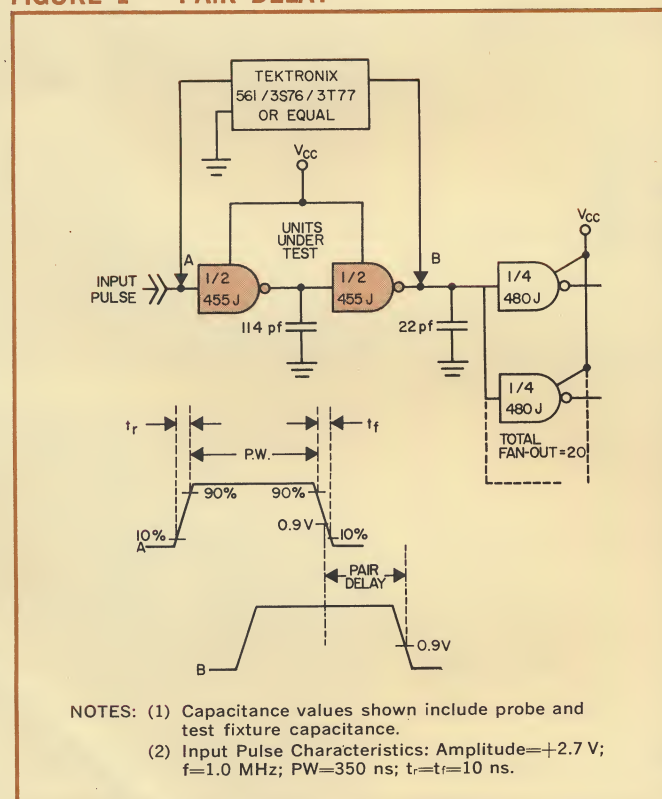
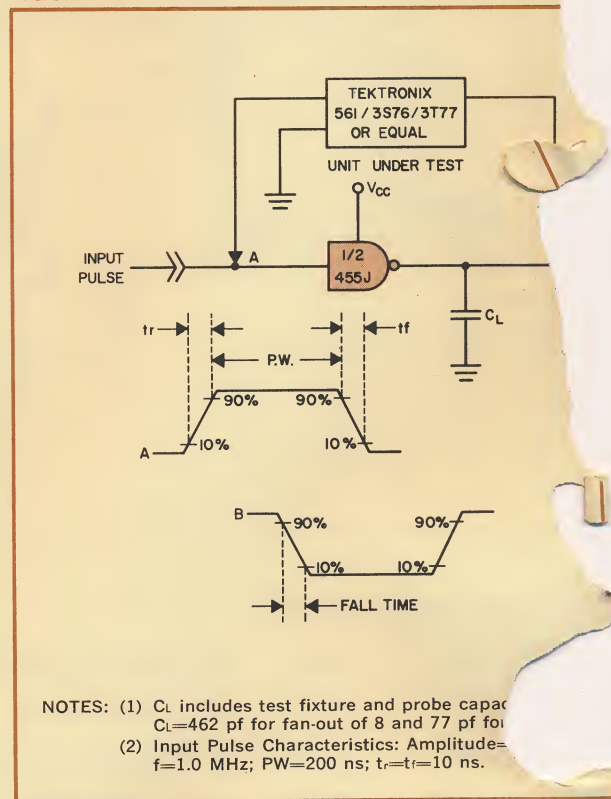


FIGURE 2 — FALL TIME



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LOW POWER MONOLITHIC TTL ELEMENT QUADRUPLE TWO-INPUT NAND GATE

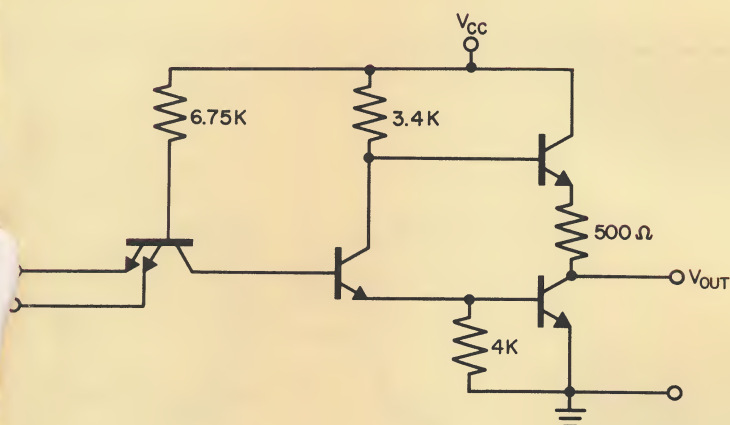
NE480J

The NE480J is a monolithic semiconductor integrated circuit designed for use in low power digital systems. This element is functionally identical to the SE480J. Full MIL range systems may be economically breadboarded using the NE480J element so long as the designer takes cognizance of the temperature differential. For GSE designs or other limited temperature range applications, the NE480J offers the opportunity to exploit, at very low cost, all of the major advantages of the SE480J. For additional data on the NE480J, see the SE480J data sheet.

The same planar and epitaxial techniques used in fabricating the SE400J-Series elements are employed in making the NE400J-Series. These elements are tested under Signetics established SURE Program (Systematic Uniformity and Reliability Evaluation), as described in Bulletin No. 5001. Acceptance Test Sub-Groups called out in the tabular data refer to selection and test criteria as specified in Table II of SURE Program Bulletin No. 5001. Please note, however, that the NE400J-Series is intended for operation in the 0°C to +70°C range.

CIRCUIT SCHEMATIC

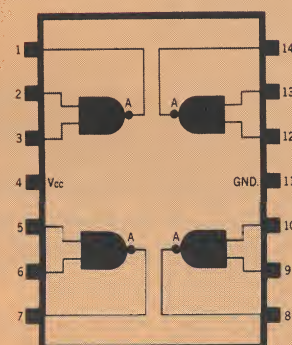
FIGURE 1: 1/4 of NE480J shown. Component values are typical.



ABSOLUTE MAXIMUM RATINGS

VOLTAGE	6.0V	OPERATING TEMP.	0°C to +70°C
STORAGE TEMP.	6.0V	STORAGE TEMP.	-65°C to +150°C
CURRENT	±10mA	θ JUNCTION TO CASE	0.2°C/mW
TEMPERATURE	+30, -10mA	JUNCTION TEMP.	150°C

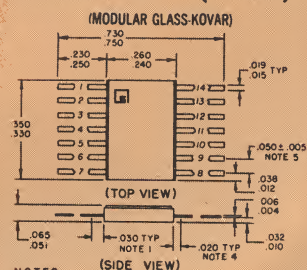
are limiting values above which serviceability may be impaired.



NOTE:

(1) A — Active pull-up

J-PACKAGE—(TO-88)



NOTES:

- (1) Recommended minimum offset before lead bend.
- (2) All leads weldable and solderable.
- (3) All dimensions in inches.
- (4) Lead spacing dimensions apply to this area only.
- (5) Spacing tolerances non-cumulative.

ELECTRICAL CHARACTERISTICS (Notes: 1, 2, 3, 4, 5, 6)

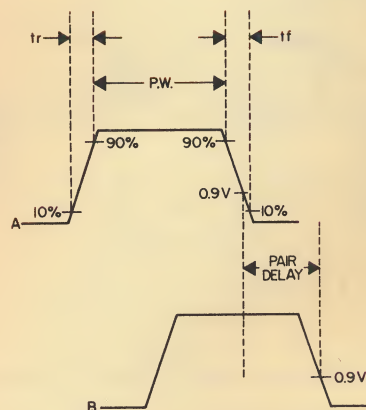
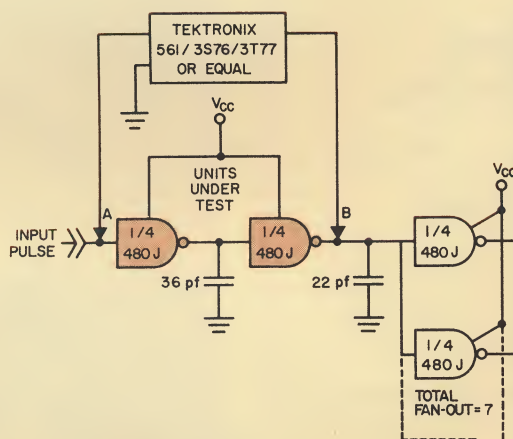
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NOTES:

- (1) All voltage and capacitance measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.
- (2) All measurements are taken with Pin 11 tied to zero volts.
- (3) Positive current flow is defined as into the terminal referenced.
- (4) Positive NAND Logic definition: "UP" Level = "1", "DOWN" Level = "0".
- (5) Precautionary measures should be taken to ensure current limiting in accordance with maximum ratings should the isolation diode is forward biased.
- (6) Measurements apply to each gate element independently.
- (7) Capacitance as measured on Bonton Electronic Corporation Model 75A-S8 Capacitance Bridge

- (9) or equivalent, $f = 1 \text{ kHz}$, $V_{ac} = 25 \text{ mV}_{\text{rms}}$. All pins not specifically referenced are tied to ground for capacitance tests.
- (10) Output leakage current is supplied through a resistor to ground.
- (11) DC fan-out is defined in terms of a SIGNETICS Standard Unit Load, which is an NE4840 gate input or an equivalent impedance.
- (12) One AC fan-out is defined as equivalent to one clock pulse input of an NE424J or a 50 pF capacitance load.
- (13) This is not a test point, but is guaranteed as a result of calculations using guaranteed test point data.
- (14) Measured at 50 percent duty cycle.

FIGURE 1 — PAIR DELAY



NOTES: (1) Capacitance values shown include probe and test fixture capacitance.
(2) Input Pulse Characteristics: Amplitude=+2.7 V; f=1.0 MHz; PW=350 ns; $t_r=t_f=10$ ns.



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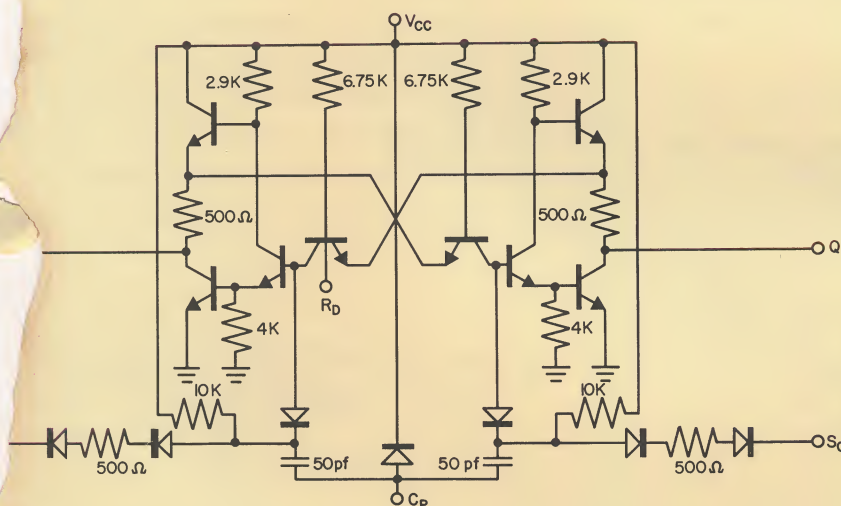
LOW POWER MONOLITHIC ELEMENT DUAL AC BINARY

The NE424J is a monolithic semiconductor integrated circuit designed for use in low power digital systems. This element is functionally identical to the SE424J. Full MIL range systems may be economically breadboarded using the NE424J element so long as the designer takes cognizance of the temperature differential. For GSE designs or other limited temperature range applications, the NE424J offers the opportunity to exploit, at very low cost, all of the major advantages of the SE424J. For additional data on the NE424J, see the SE424J data sheet.

The same planar and epitaxial techniques used in fabricating the SE400J-Series elements are employed in making the NE400J-Series. These elements are tested under Signetics established SURE Program (Systematic Uniformity and Reliability Evaluation), as described in Bulletin No. 5001. Acceptance Test Sub-Groups called out in the tabular data refer to selection and test criteria as specified in Table II of SURE Program Bulletin No. 5001. Please note, however, that the NE400J-Series is intended for operation in the 0°C to +70°C range.

CIRCUIT SCHEMATIC

NOTE: 1/2 of NE424J shown. Component values are typical.

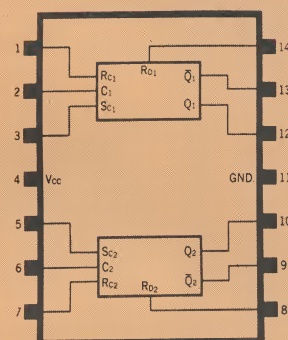


ABSOLUTE MAXIMUM RATINGS

VOLTAGE	6.0V	OPERATING TEMP.	0°C to +70°C
	6.0V	STORAGE TEMP.	-65°C to +150°C
CURRENT	±10mA	θ JUNCTION TO CASE	0.2°C/mW
OUTPUT CURRENT	+30, -10mA	JUNCTION TEMP.	150°C

These ratings are limiting values above which serviceability may be impaired.

NE424J

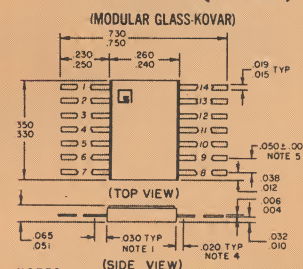


TRUTH TABLE

R_C	S_C	Q_{N+1}
1	0	1
0	1	0
1	1	No Change
0	0	?

$R_D = 0 \Rightarrow Q = 0$

J-PACKAGE—(TO-88)



NOTES:

- (1) Recommended minimum offset before lead bend.
- (2) All leads weldable and solderable.
- (3) All dimensions in inches.
- (4) Lead spacing dimensions apply to this area only.
- (5) Spacing tolerances non-cumulative.

ELECTRICAL CHARACTERISTICS (Notes: 1, 2, 3, 4, 5, 6)

ACCEPTANCE TEST SUB-GROUP	CHARACTERISTIC	LIMITS				TEST CONDITIONS							
		MIN.	TYP.	MAX.	UNITS	TEMP.	V _{cc}	R _D	CLOCK	S _C	R _C	OUTPUT	NOTES
A-5 A-3 A-4	"1" OUTPUT VOLTAGE Q, $\bar{Q}$	2.5 2.5 2.5			V	0°C +25°C +70°C	4.0V 4.0V 4.0V	0.8V 0.8V 0.8V				-140μA -140μA -140μA	
A-5 A-3 A-4	"0" OUTPUT VOLTAGE Q, $\bar{Q}$			0.32 0.32 0.32	V	0°C +25°C +70°C	4.0V 4.0V 4.0V	1.7V 1.7V 1.7V				5.6mA 5.6mA 5.6mA	
A-5 A-3 A-4 A-5 A-3 A-4 A-3	"0" INPUT CURRENT												
A-5 A-3 A-4	R _D	-0.34		-0.8	mA	0°C +25°C +70°C	4.0V 4.0V 4.0V	0V 0V 0V					
A-5 A-3 A-4	S _C , R _C	-0.15		-0.5	mA	0°C +25°C +70°C	4.0V 4.0V 4.0V			0V 0V 0V	0V 0V 0V		
A-3	CLOCK			-250	nA	+25°C	4.0V		0V				
A-4 A-4	"1" INPUT CURRENT			20 10	μA	+70°C +70°C	4.0V 4.0V	4.0V					
	TURN-ON DELAY (Figure 1)		46		ns	+25°C	4.0V			4.0V	4.0V	F.O.=7	10
	TURN-OFF DELAY (Figure 1)		43		ns	+25°C	4.0V					F.O.=7	10
	AVERAGE POWER CONSUMPTION Per Binary		9.7		mW	+25°C	4.0V			Q	$\bar{Q}$		12
C-2	TOGGLE SPEED	5.0			MHz	+25°C	4.0V			Q	$\bar{Q}$		
C-2	OUTPUT FALL TIME (Figure 2)			75	ns	+25°C	4.0V					AC F.O.=2	11
	INPUT CAPACITANCE												
	CLOCK		50		pf	+25°C	4.0V		2.0V				7
	R _D		3.0		pf	+25°C	4.0V	2.0V					7
	S _C , R _C		3.0		pf	+25°C	4.0V			2.0V	2.0V		7
A-2	INPUT VOLTAGE RATING												
	R _D		6.0		V	+25°C	4.0V	10μA					
	CLOCK		4.3		V	+25°C	4.0V		10μA	0V	0V		
	DC FAN-OUT		7										10
	AC FAN-OUT		2										11

NOTES:

- (1) All voltage and capacitance measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.
- (2) All measurements are taken with Pin 11 tied to zero volts.
- (3) Positive current flow is defined as into the terminal referenced.
- (4) Positive NAND Logic definition: "UP" Level = "1", "DOWN" Level = "0".
- (5) Precautionary measures should be taken to ensure current limiting in accordance with maximum ratings should the isolation diodes become forward biased.
- (6) Measurements apply to each binary element independently.
- (7) Capacitance as measured on Bonton Electronic Corporation Model 75A-S8 Capacitance Bridge

- (8) The binary Q side is set in a "1" by clocking once with the R_C line high and the S_C line low, alternate $\bar{Q}$ test S_C is set high, R_C low and the binary clocked once.
- (9) Output leakage current is supplied through a resistor to ground.
- (10) DC fan-out is defined in terms of a SIGNETICS Standard Unit Load, which is an NE480J gate in an equivalent impedance.
- (11) One AC fan-out is defined as equivalent to one clock pulse input of an NE424J or a 50 pf capacitance.
- (12) Measured at 50 percent duty cycle.

FIGURE 1 — CLOCKED MODE TURN ON AND TURN OFF DELAY

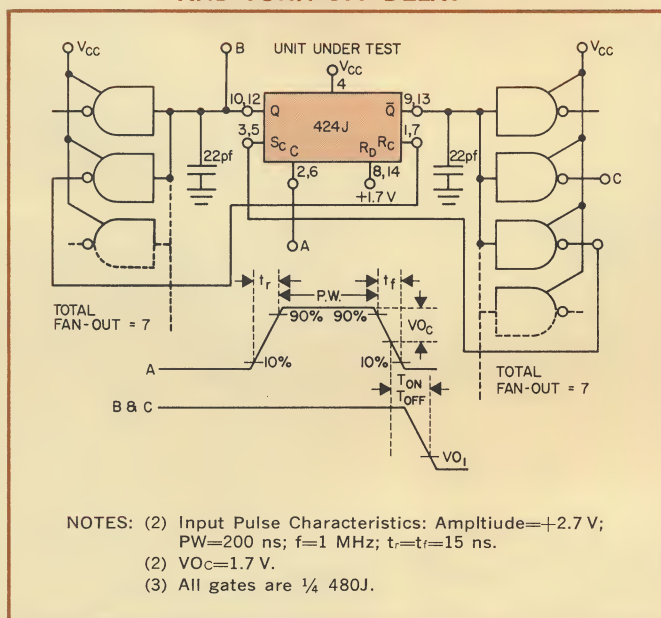
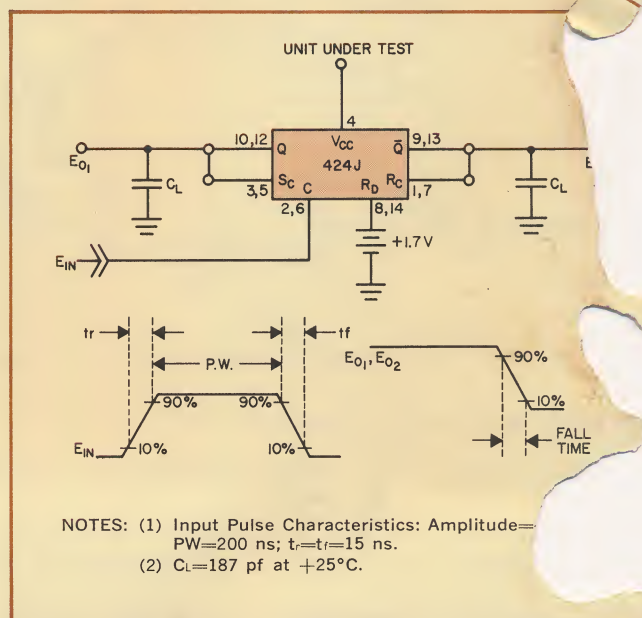


FIGURE 2 — OUTPUT FALL TIME CIRCUIT



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